PATENT ABSTRACTS OF JAPAN

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(54) **SOLID-STATE IMAGE PICKUP DEVICE**

(57)Abstract:
PROBLEM TO BE SOLVED: To prevent an excess rush current caused when all picture elements of the solid-state image pickup device are reset.
SOLUTION: The solid-state image pickup device having plural pixels for photoelectric conversion and scanning circuits 59 selecting sequentially the plural picture elements 1 is provided with a shift register as a scanning circuit to set outputs of plural circuit stages to a prescribed logic state nearly simultaneously and with a light receiving element PD as a picture element 1 and an amplifier element QA amplifying a signal charge stored in the light receiving element PD. Outputs of plural circuit stages of the shift register of the scanning circuit 5 are set to the prescribed logic state to select plural picture elements 1 and the charge of the light receiving element PD is reset while the plural selected picture elements 1 cut off the amplifier element QA.

CLAIMS

[Claim(s)]
[Claim 1]Two or more pixels which perform photoelectric conversion.
A scanning circuit for choosing said two or more pixels one by oneand reading them.
Are the above the solid state camera which it hadand said scanning circuitTandem connection of two or more circuit

stages is carried outthey are constitutedand it has a shift register which can be set as a predetermined logic state almost simultaneous for an output of two or more of said circuit stages according to an input of a predetermined control signalA photo detector in which said pixel accumulates a signal charge according to a lightwave signal at least respectivelyWhile choosing two or more pixels by having an amplifier which amplifies a signal charge accumulated in this photo detectorand setting an output of two or more circuit stages of a shift register of said scanning circuit as said predetermined logic stateRush current at the time of reset was reduced by resetting an electric charge of said photo detectorwhere said amplifier is cut off in two or more selected pixels.

[Claim 2]Transfer elements which transmit a signal charge [each / of said pixel] further accumulated in said photo detector to a control electrode of said amplifierThe solid state camera according to claim 1 providing a reset element which resets an electric charge of a control electrode of said amplifierand resetting an electric charge of a photo detector by considering both said transfer elements and said reset element as one.
[Claim 3]The solid state camera according to claim 2 including a bias voltage applying means for impressing bias voltage to said amplifier and holding said amplifier in the cutoff statewhen resetting an electric charge of a photo detector by considering both said transfer elements and a reset element as one.
[Claim 4]Two or more pixels which consist of an amplified type photoelectric conversion means which is arranged in the shape of two dimensions in a line and a line directionand accumulates and amplifies a signal charge according to a lightwave signal respectivelyIn a current regulator circuit provided for each [which connected in common an output terminal of each pixel arranged in a line direction] sequence line of everyand a solid state camera which carry out selection driving of said pixel and which is level and has vertical each scanning circuitTandem connection of two or more circuit stages is carried outthey are constitutedand said vertical scanning circuit is provided with a shift register which can be set as a predetermined logic state for an output of two or more of said circuit stages almost simultaneous according to an input of a predetermined control signalA photo detector in which said pixel accumulates a signal charge according to a lightwave signal respectivelyand an amplifier which

amplifies a signal charge accumulated in this photo detectorTransfer elements which transmit a signal charge accumulated in said photo detector to a control electrode of said amplifierA reset element which resets an electric charge of a control electrode of said amplifier is providedA control electrode of transfer elements of a pixel of each line is connected to a row line corresponding in commona row line of each line is connected to correspondence circuit stages of said vertical scanning circuitand a control electrode of a reset element of all the pixels is connected to a reset control signal input terminal in commonAnd all the transfer elements are considered as one via said each row line by setting an output of two or more circuit stages of a shift register of said vertical scanning circuit as said predetermined logic stateAnd while considering a reset element of all the pixels as one and resetting an electric charge of a photo detector via transfer elements and a reset element by adding said reset control signal to a reset element of all the pixelsA solid state camera reducing rush current at the time of reset by impressing voltage which changes this amplifier into a cutoff state to a control electrode of an amplifier via a reset element which became one on the occasion of this reset.

[Claim 5]Two or more pixels which consist of an amplified type photoelectric conversion means which is arranged in the shape of two dimensions in a line and a line directionand accumulates and amplifies a signal charge according to a lightwave signal respectivelyIn a current regulator circuit provided for each [which connected in common an output terminal of each pixel arranged in a line direction] sequence line of everyand a solid state camera which carry out selection driving of said pixel and which is level and has vertical each scanning circuitTandem connection of two or more circuit stages is carried outthey are constitutedand said vertical scanning circuit is provided with a shift register which can be set as a predetermined logic state for an output of two or more of said circuit stages almost simultaneous according to an input of a predetermined control signalA photo detector in which said pixel accumulates a signal charge according to a lightwave signal respectivelyand an amplifier which amplifies a signal charge accumulated in this photo detectorTransfer elements which transmit a signal charge accumulated in said photo detector to a control electrode of said amplifierA reset element which resets an electric charge of a control electrode of said amplifier is

providedIn commona control electrode of transfer elements of a pixel of each line is connected to a row line corresponding in commona row line of each line is connected to correspondence circuit stages of said vertical scanning circuitand a control electrode of a reset element of all the pixels is connected to a reset control signal input terminaland each sequence lineIt has a means to impress bias voltage to an amplifier via each sequence line in order to change into a cutoff state an amplifier of a pixel connected to each sequence lineAnd all the transfer elements are considered as one via said each row line by setting an output of two or more circuit stages of a shift register of said vertical scanning circuit as said predetermined logic stateAnd while considering a reset element of all the pixels as one and resetting an electric charge of a photo detector via transfer elements and a reset element by adding said reset control signal to a reset element of all the pixelsA solid state camera reducing rush current at the time of reset by changing an amplifier of all the pixels into a cutoff state by said bias voltage applying means in the case of this reset.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Concerning a solid state camerathis invention is used for an electronic "still" camera etc.and relates to the solid state camera which instant reset of all the pixels is possibleand can moreover reduce the rush current at the time of reset substantially.
[0002]
[Description of the Prior Art]Drawing 6 shows the composition of the outline of the conventional solid state cameraand shows the example of the two-dimensional image sensor. The equipment of the figure is made into the pixel configuration of three lines x three rows for simplification of explanation. Although the subscript is given to the reference mark of each element in Drawingsa subscript may be omitted when expressing on behalf of the same kind of element for simplification of explanation.
[0003]With the equipment of drawing 6the static induction transistor (SIT) is used as an example of an amplified type photo detector as each pixel. That isstatic-induction-transistor QS11 which constitutes each pixelQS12QS13QS21QS22QS23QS31QS32and QS33 are arranged at

the matrix form of three lines x three rows.
[0004]The vertical scanning circuit VSR for choosing the pixel of each sequence one by one for every line is formed. That isthe gate of the static induction transistor arranged among the pixels arranged at matrix form at each line writing direction is connected to each circuit stages of the shift register of the vertical scanning circuit VSR via each row line GV1GV2and GV3 in common. For examplethe gate of static-induction-transistor QS11QS12and QS13 is connected to the vertical scanning circuit VSR via row line GV1 bothand the gate of each static-induction-transistor QS21QS22and QS23 is connected to the vertical scanning circuit VSR via row line GV2. All the circuit stages are reset or preset by impression of initializing signal phiINTVand the vertical scanning circuit VSR can make the selective state all the row line GV1GV2and GV3 by it.
[0005]The source of the static induction transistor of the pixel of each sequence is connected common to sequence line LV1 of the sequenceLV2and LV3and each sequence line is connected to the predetermined power supply VEE via constant current source CSV. Each constant current source CSV serves as load of the static induction transistor QS of each pixel at the time of signal read-out from each pixel. The drain of the static induction transistor QS of each pixel is connected to the predetermined power supply VDD in common. The end of each sequence line LV1LV2and LV3 is grounded via transistor QRSTV1 for vertical reset for resetting each sequence lineQRSTV2and QRSTV3. Reset-signal phiRSTV for vertical read-out lines explained later is supplied to each transistor for vertical reset.
[0006]The other end of each sequence line LV1LV2and LV3 is connected to the drain of each transistor QH1 for a level outputQH2and QH3 via each switch QT1 for transmissionQT2and QT3. The source of each transistor for a level output is connected to the common level output line HOUTand this level output line HOUT is connected to the video output terminal for supplying an imaging signal outside. The source of each transistor QT1 for transmissionQT2and QT3 is grounded via each capacity CT1CT2and CT3.
[0007]The gate of transistor QT1 for transmission of each sequenceQT2and QT3 is connected in commonand transfer pulse phiT is supplied. The gate of the level read transistors QH1-QH3 is connected to each circuit stages of the horizontal scanning circuit HSR. The horizontal scanning circuit HSR as well as said vertical scanning circuit VSR is provided with a shift registerandas for this shift registerthe thing in which the set or reset of all the

circuit stages is possible is used by level initializing signal phiINTH.
[0008]When usedfor example for an electronic "still" camerathe solid state camera of drawing 6By adding vertical start signal phiSTV to the vertical scanning circuit VSRand adding clock signal phiCKV for vertical shifts after progress of predetermined exposure timeit operates so that the shift register of the vertical scanning circuit VSR may shift said start signal phiSTV to each circuit stages one by one. Each row line GV1GV2and GV3 are chosen one by one by this. The signal charge according to incident light is accumulated in each static induction transistor QSThis static induction transistor outputs the voltage corresponding to the electric charge which operated as a source follower and was accumulated to each sequence line LV by applying predetermined selection voltage to the gate voltage in the selected line. That isthe signal from the static induction transistor QS of the selected line is simultaneously outputted to each vertical read-out line LV.
[0009]And QT is interceptedafter carrying out conduction of the transfer transistor QT of each sequence by transfer signal phiT at this time and charging a signal charge capacity CT1CT2and CT3The signal for every sequence is outputted to the level output line HOUT by considering the level read transistor QH as one one by one by the vertical scanning circuit HSR.
[0010]By the waywhen such a solid state camera is usedfor example for an electronic "still" cameraafter resetting all the pixels at the moment of pushing a shutterthe image pick-up of an object image is performed. In the solid state camera of drawing 6reset of all the pixels is performed as follows.
[0011]That isthe vertical scanning circuit VSR is controlled by initializing signal phiINTVclock signal phiCKVand scanning start signal phiSTV including a shift register. If initializing signal phiINTV and phiSTV are made into a highall the circuit stages of the vertical scanning circuit VSR will be presetall the row line GV1GV2and GV3 will become a highand all the pixels will be in a selective state. On the other handif initializing signal phiINTV is made into a high and scanning start signal phiSTV is made into a loweach circuit stages of the vertical scanning circuit VSR are resetand all the pixels will be in a non selection state. If initializing signal phiINTV is made into a lowthe vertical scanning circuit VSR will start the usual shift actionwhenever clock signal phiCKV enters from the time of start signal phiSTV becoming

a higheach row line GV1GV2and GV3 are set to a high level one by oneand the pixel of one line is chosen at a time one by one.
[0012]And in order to reset all the pixels in the solid state camera of drawing 6vertical read-only reset-signal phiRSTV is first made into a highthe transistor QRSTV 1-3 for vertical reset of each sequence is considered as oneand each sequence line LV1LV2and LV3 are connected to a ground.
[0013]Nextboth said initializing signal phiINTV of the vertical scanning circuit VSR and scanning start signal phiSTV are made into a highand each circuit stages of the vertical scanning circuit VSR are changed into a preset state. By thisboth each row line GV1GV2and GV3 will become high-leveland they will be in the selective state of all the pixels. The high-level voltage of each row line GV1 in this caseGV2and GV3i.e.the voltage of control signal phiSRs 1-3is set up become the voltage VRSTP for reset of the static induction transistor QS 11-33.
[0014]As everyone knowsan inversion layer is formed in the gate electrode lower part of each static inductions transistor QS11-QS33 of thisand a channel can be done by it between the source drains of this static induction transistor QS 11-33The remaining charge charged at the gate flows outand reset of all the pixels is performed. At this timethe current by the outflow of the remaining charge by reset flows into the static inductions transistor QS11-QS33 of each pixel simultaneously.
[0015]
[Problem to be solved by the invention]Thusin the solid state camera which has the conventional amplified type image sensorwhen all the pixels were resetit was resetting by choosing all the pixels simultaneously by making into one a picture element part including an amplifying means. For this reasonat the time of resetall the amplifying means in each pixel are also turned on simultaneouslyand the current of all the amplifying means flows all at once. Although the current at this time is called rush currentsince all the pixels become small with one simultaneouslybig rush current flows through the rush current of each pixel with the whole imaging device.
[0016]For examplethough the rush current of each pixel is several microamperewhen a pixel number is 1 million pixelsin the whole imaging deviceit amounts to several amperes. If the current which amounts to several amperes flows into the chip of a solid state camerathe fall of the reliability by electromigration will become a problemThere was also a possibility of the voltage of each [in a chip]

portion not having fitted in a predetermined voltage range with the parasitism impedance of each portion in a chipand the performance which the chip expected as a solid state camera not having been demonstratedor producing malfunction by rush currentetc.
[0017]Thereforein the solid state camera which uses an amplified type pixel in view of a problem [in / in the purpose of this invention / such conventional equipment]Prevent the excessive rush current at the time of resetand the whole chip of a solid state camera enables it to demonstrate predetermined performanceand it is in enabling it to also prevent the fall of the reliability of a solid state camera exactly.
[0018]
[Means for solving problem]In a solid state camera possessing a scanning circuit for according to the 1st aspect of this inventionchoosing two or more pixels which perform photoelectric conversionand said two or more pixels one by oneand reading themin order to attain the above-mentioned purposeTandem connection of two or more circuit stages should be carried outthey should be constitutedand said scanning circuit should be provided with a shift register which can be set as a predetermined logic state for an output of two or more of said circuit stages almost simultaneous according to an input of a predetermined control signal. A photo detector in which said pixel accumulates a signal charge according to a lightwave signal at least respectivelyWhile choosing two or more pixels by having had an amplifier which amplifies a signal charge accumulated in this photo detectorand setting an output of two or more circuit stages of a shift register of said scanning circuit as said predetermined logic stateRush current at the time of reset is reduced by resetting an electric charge of said photo detectorwhere said amplifier is cut off in two or more selected pixels.
[0019]In such compositionwhere said amplifier is cut off in two or more pixels which chose and chose two or more pixels with a shift register of said scanning circuitan electric charge of said photo detector is reset. Thereforeit is lost that rush current flows into an amplifier at the time of resetand even if it resets simultaneously all the pixels in a solid state camera which has many pixelsit is lost that excessive rush current flows. Thereforethe reliability of a solid state camera does not falland it becomeswithout moreover voltage of each portion in a chip of a solid state camera causing a big change by rush currentand a solid state camera can demonstrate original performance now

exactly.
[0020]In this casethe transfer elements which transmit the signal charge [each / of said pixel] further accumulated in said photo detector to the control electrode of said amplifierThe reset element which resets the electric charge of the control electrode of said amplifier shall be providedand the electric charge of a photo detector shall be reset by considering both said transfer elements and said reset element as one.
[0021]By applying the voltage which considers said transfer elements and a reset element as one at both the times of resetand cuts off this amplifier to the control electrode of an amplifier via a reset element by taking such a pixel configurationIt becomes possible to emit the electric charge accumulated in the photo detector via said transfer elements and a reset elementwhere an amplifier is cut off.
[0022]When resetting the electric charge of a photo detector by considering both said transfer elements and a reset element as oneit can also constitute so that the bias voltage applying means for impressing bias voltage to said amplifier and holding said amplifier in the cutoff state may be included.
[0023]In this casethe bias voltage for changing said amplifier into a cutoff state to said amplifier at the time of reset of a pixel by the above-mentioned bias voltage applying means can be impressed. Thereforethe characteristic of a photo detector and an amplifier can be set as the independently optimal respectively thingwhere an amplifier is cut off thoroughlyperfect depletion-ization of a photo detector can be attainedthe flexibility of a design of each element increasesand a quality solid state camera can be realized.
[0024]Two or more pixels which consist of an amplified type photoelectric conversion means which is arranged in the shape of two dimensions in a line and a line directionand accumulates and amplifies the signal charge according to a lightwave signal respectively in other aspects of this inventionIn the current regulator circuit provided for each [which connected in common the output terminal of each pixel arranged in the line direction] sequence line of everyand the solid state camera which carry out selection driving of said pixel and which is level and has vertical each scanning circuitTandem connection of two or more circuit stages should be carried outthey should be constitutedand said vertical scanning circuit should be provided with the shift register which can be set as a predetermined logic state for the output of two or more of

said circuit stages almost simultaneous according to the input of a predetermined control signal. Said pixel respectively the signal charge according to a lightwave signal. The photo detector to accumulatethe amplifier which amplifies the signal charge accumulated in this photo detectorthe transfer elements which transmit the signal charge accumulated in said photo detector to the control electrode of said amplifierand the reset element which resets the electric charge of the control electrode of said amplifier are providedThe control electrode of the transfer elements of the pixel of each line is connected to a row line corresponding in commonthe row line of each line is connected to the correspondence circuit stages of said vertical scanning circuitand the control electrode of the reset element of all the pixels is connected to a reset control signal input terminal in commonAnd all the transfer elements are considered as one via said each row line by setting the output of two or more circuit stages of the shift register of said vertical scanning circuit as said predetermined logic stateAnd while considering the reset element of all the pixels as one and resetting the electric charge of a photo detector via transfer elements and a reset element by adding said reset control signal to the reset element of all the pixelsBy impressing the voltage which changes this amplifier into a cutoff state to the control electrode of an amplifier via the reset element which became one on the occasion of this resetthe rush current at the time of reset is reduced.

[0025]In the solid state camera concerning such compositionAt the time of resetall the transfer elements of each row line are considered as one by making the output of two or more circuit stages of the shift register of said vertical scanning circuit into a predetermined logic stateAnd the reset element of all the pixels can be considered as oneand the electric charge of a photo detector can be reset via transfer elements and a reset element. If the voltage which changes this amplifier into a cutoff state is impressed to the control electrode of an amplifier via the reset element which became one on the occasion of this resetIt is lost that rush current flows into an amplifier at the time of resetand even if it resets many pixels simultaneouslyit is lost that rush current excessive as the whole solid state camera flows.

[0026]In the aspect of further others of this invention. The current regulator circuit provided for each [which connected in common the output terminal of two or more pixels which consist of an amplified type photoelectric

conversion means which is arranged in the shape of two dimensions in a line and a line directionand accumulates and amplifies the signal charge according to a lightwave signal respectivelyand each pixel arranged in the line direction] sequence line of everyand said pixel. In the solid state camera which carries out selection driving and which is level and has vertical each scanning circuitTandem connection of two or more circuit stages should be carried outthey should be constitutedand said vertical scanning circuit should be provided with the shift register which can be set as a predetermined logic state for the output of two or more of said circuit stages almost simultaneous according to the input of a predetermined control signal. Said pixel respectively the signal charge according to a lightwave signal. The photo detector to accumulatethe amplifier which amplifies the signal charge accumulated in this photo detectorthe transfer elements which transmit the signal charge accumulated in said photo detector to the control electrode of said amplifierand the reset element which resets the electric charge of the control electrode of said amplifier are providedThe control electrode of the transfer elements of the pixel of each line is connected to a row line corresponding in commonthe row line of each line is connected to the correspondence circuit stages of said vertical scanning circuitand the control electrode of the reset element of all the pixels is connected to a reset control signal input terminal in commonIt has a means to impress bias voltage to an amplifier via each sequence line in order that each sequence line may change into a cutoff state the amplifier of the pixel connected to each sequence lineAnd all the transfer elements are considered as one via said each row line by setting the output of two or more circuit stages of the shift register of said vertical scanning circuit as said predetermined logic stateAnd while considering the reset element of all the pixels as one and resetting the electric charge of a photo detector via transfer elements and a reset element by adding said reset control signal to the reset element of all the pixelsBy changing the amplifier of all the pixels into a cutoff state by said bias voltage applying means in the case of this resetthe rush current at the time of reset is reduced. [0027]All the transfer elements are considered as one via each row line by setting an output of two or more circuit stages of a shift register of a vertical scanning circuit as a predetermined logic state also in this caseAnd by considering a reset element of all the pixels as one with said reset control signalan electric charge of a photo

detector can be emitted via transfer elements and a reset element. And rush current at the time of reset can be reduced by changing an amplifier of all the pixels into a cutoff state by said bias voltage applying means in the case of this reset. Since said bias voltage applying means can impress desired suitable bias voltage to an amplifier of a pixel independently with other elementsit can increase flexibility of a design of each element of a pixel. Namelya photo detector can supply voltage depletion-ized thoroughly via said transfer elements and a reset elementOn the other handbias voltage which fully changes this amplifier into a cutoff state can be independently impressed to said amplifierand it can design have the optimal characteristic of respectively a request of a photo detector and an amplifier.

[0028]

[Mode for carrying out the invention]Drawing 1 is a block diagram showing composition of an outline of a solid state camera concerning this inventionand shows an example of a two-dimensional image sensor. A solid state camera of the figure is provided with the following.

The picture element part 3 which has two or more pixels 1.

The vertical scanning circuit 5.

The level read section 7.

The horizontal scanning circuit 9.

[0029]The pixel 1 provided with a photo-diodean amplifieretc. for light-receiving so that it might explain in detail laterrespectively is arranged at matrix formand the picture element part 3 is constituted. The vertical scanning circuit 5 chooses the pixel for 1 horizontal line (row line) of the picture element part 3 one by oneand comprises a dynamic shift register of structure who shows later. The level read section 7 accepts the electric charge of the pixel for 1 horizontal line from the picture element part 3and outputs this one by one based on the scanning pulse from the horizontal scanning circuit 9. The horizontal scanning circuit 9 is also constituted by the same dynamic shift register as said vertical criminal-investigation circuit 5.

[0030]Signal phiSTV inputted into the vertical scanning circuit 5 is a vertical start pulseand serves as a dynamic shift register's initial input data. Vertical clock pulse phiCKV for shifting the dynamic shift register and vertical initialization-pulses phiINTV are inputted into the vertical scanning circuit 5.

[0031]Signal phiSTH inputted into the horizontal scanning

circuit 9 is a start signal of the dynamic shift register who constitutes the horizontal scanning circuit 9and phiCKH is a clock signal for a level shift. Level initialization-pulses phiINTH for initializing the dynamic shift register who constitutes this horizontal scanning circuit 9 if needed is inputted into the horizontal scanning circuit 9.
[0032]In the solid state camera of drawing 1when usedfor example for a still video camera etc.before pushing a shuttera solid state camera carries out false operationnamelya scan is carried outbut the output signal is changed into the state where it is not used. And if a shutter is pushedfixed time initialization-pulses phiINTV for about 10 microseconds will be added to the vertical scanning circuit 5 and start pulse phiSTV will be simultaneously used as H levelThe whole page of the shift register of the vertical scanning circuit 5 under false operation will be in a preset state compulsorilyall the pixels will be in a selective stateand the electric charge of all the pixels can be reset.
[0033]Nextuse vertical start pulse phiSTV as L leveland the vertical scanning circuit 5 is made into a reset stateAnd after adding initialization-pulses phiINTH also to the horizontal scanning circuit 9and using horizontal start pulse phiSTH as L level and making the horizontal scanning circuit 9 into a reset stateit returns to normal operation and the shift action of each shift register is started. At this timeeach pixel has started accumulation of picture informationand again initialization-pulses phiINTV and phiINTH after progress of predetermined exposure time H levelIf it returns to the usual operation and reading operation is started after using vertical start pulse phiSTV and horizontal start pulse phiSTH as L level and carrying out forcible reset of each shift registerthe predetermined video signal by which time exposure was carried out can be obtained.
[0034]The read operation usual in the solid state camera of drawing 1In the state where it was considered as the lowrespectivelyeach initialization-pulses phiINTV of the vertical scanning circuit 5 and the horizontal scanning circuit 9and phiINTH. In the vertical scanning circuit 5start signal phiSTV of a high level is shifted one by one by clock signal phiCKVand the pixel for 1 horizontal line of the picture element part 3 is chosen one by one. The electric charge accumulated in the photo-diode of each pixel for selected 1 horizontal line is transmitted to the level read section 7. Nextby the horizontal scanning circuit 9by shifting start signal phiSTH of a high level

one by one by clock signal phiCKHthe electric charge transmitted to the level read section 7 by this horizontal scanning circuit 9 is horizontally transmitted one by one by 1 pixeland it reads outside from an output terminal.
[0035]Drawing 2 shows the detailed circuitry of the solid state camera of drawing 1. The same portion as drawing 1 is shown by the same reference number in the solid state camera of drawing 2. That isthe solid state camera of drawing 2 is also constituted by the picture element part 3 provided with two or more pixels 1the vertical scanning circuit 5the level read section 7the horizontal scanning circuit 9etc. In the circuit of drawing 2the picture element part 3 shall comprise the pixel 1 of three lines x three rows for simplification of explanation.
[0036]Photo-diode PD in which each pixel 1 is a photo detectoramplifier QA which consists of junction field effect transistors (JFET)It comprises the reset switch QRST which consists of a MOS transistor for setting the gate electrode of the switch QT for transmission which consists of a MOS transistor for transmitting the electric charge of photo-diode PD to the gate of amplifier QAand amplifier QA as predetermined voltage. In Drawingsalthough the subscript is made each elementwhen expressing on behalf of the same kind of element for simplification of explanationa subscript may be omitted. In each pixel 1 shown in drawing 2the gate of photo-diode PD which is a euphotic meansand amplifier QA is separated on structure.
[0037]The source of amplifier QA of the pixel perpendicularly arranged among amplifier QA of each pixel 1 is connected to constant current source CSV of each sequence via sequence line LV (LV1-LV3) of each sequence. Each constant current source CSV serves as load when operating amplifier QA as a source follower. The other end of each constant current source CSV is connected to the predetermined power supply VEE in common.
[0038]The cathode of photo-diode PD of each pixel 1 is connected to the predetermined power supply VDD in commonand the anode is connected to the source of the switch QT for transmission. The drain of the switch QT for transmission is connected to the gate of amplifier QAand the source of the reset switch QRST. The source of each amplifier QA is connected to each sequence line LV (LV1-LV3) in common for every sequence. The gate of each switch QT for transmission is constituted so that it may be connected to the vertical scanning circuit 5 in common for every line and 1st vertical-scanning-signals phiTR may be received. Vertical-scanning-signals phiTR1 of each line -

phiTR3 are connected to the output of each circuit stages of the vertical scanning circuit 5.The gate of the reset switch QRST is connected to control signal phiPG [all the / pixel]and the drain is constituted so that it may be horizontally connected to the vertical scanning circuit 5 in common and 2nd vertical-scanning-signals phiRD may be supplied for every line. The drain of each amplifier QA is connected to the power supply VDD same in common as the anode of said photo-diode PD.

[0039]Since the output of each circuit stages of the vertical scanning circuit 5 supplies the 1st [of a voltage level]and 2nd vertical-scanning-signals phiTR(s) differentrespectively and phiRDit can also connect and constitute a predetermined voltage shift circuit in the output of each circuit stages of a shift registerrespectivelyfor example.

[0040]The level read section 7 is read for every sequenceand comprises gate-transistors QTCa capacity CTand the switch element QH for level read-out. The upper bed of each sequence line LV is connected to the drain of read-out gate-transistors QTCand the source of this read-out gate-transistors QTC is connected to the drain and capacity CT of the switch element QH for level read-out of each sequence. The other end of capacity CT is grounded. The gate of all the read-out gate-transistors QTC is constituted so that it may be connected in common and transfer pulse phiT can be supplied. The gate of the switch element QH for level read-out is connected to the output of each circuit stages of the shift register of the horizontal scanning circuit 9 for every sequence. The source of the switch element QH for level read-out is connected to the video output terminal via the level output line HOUT in common.

[0041]In the solid state camera which has the above compositionreset of a pixel is performed as follows. That isboth initialization-pulses phiINTV of the vertical scanning circuit 5 and start pulse phiSTV are made into a highall the circuit stages of the vertical scanning circuit 5 are presetand it is considered as the selective state of all the pixels. By thisall (phiTR1-phiTR3) of 1st vertical-scanning-signals phiTR of all the circuit stages are simultaneously made into a highand the switch QT for transmission of all the pixels is considered as one. Reset control signal phiPG common to all the pixels is addedand the reset switch QRST of all the pixels is made one.

[0042]Let voltage of 2nd vertical-scanning-signals phiRD (phiRD1-phiRD3) be the voltage VGL which JFET which

constitutes amplifier QA of each pixel cuts off at this time.
[0043]when it does in this waythe residual charge accumulated in photo-diode PD of each pixel is discharged through the transfer elements QT and reset element QRSTand photo-diode PD is perfect -- depletion -- it is-izing and reset. And since the gate voltage of amplifier QA is VGL as mentioned abovetherefore this amplifier QA has cut off in this casecurrent does not flow into this amplifier QA. That isthe current which the current which flows into photo-diode PD was amplified by amplifier QAand was amplified does not flow. For this reasonthe rush current of each pixel becomes very smalland it is lost that rush current excessive as the whole solid state camera flows.
[0044]Make initialization-pulses phiINTV of the vertical scanning circuit 5 into a low leveland start pulse phiSTV is made into a highand clock signal phiCKV is added and the shift action of the vertical scanning circuit 5 is made to performwhen reading a signal in the solid state camera of drawing 2. The signal which chooses the pixel of each line one by oneand is accumulated in the selected pixel by this is outputted to vertical read-out line LV. And read-out gate-transistors QTC connected to each sequence line is considered as one by transfer pulse phiTand the read-out electric charge of a signal is charged at capacity CT of each sequence. A shift action is made to perform also in the horizontal scanning circuit 9 by making a low level and start pulse phiSTH high-level for initialization-pulses phiINTHand adding clock signal phiCKH. The switch element QH for level read-out of each sequence is considered as one one by oneand the read signal of each sequence is supplied to level output line HOUT by thisand is outputted outside from a video output terminal.
[0045]In reading such a signalit makes one reset element QRST of all the pixels by reset control signal phiPG. And to the selected linevoltage of 2nd vertical-scanning-signals phiRD is made into the voltage VGH which amplifier QA of each pixel is turned on and activatesand it is considered as said voltage VGL which amplifier QA cuts off to a non selection pixel. In this stateeven if it turns OFF said control signal phiPGthe gate voltage of this amplifier QA is held with the gate stray capacitance of amplifier QA at the same value. Thereforeafter turning OFF reset element QRST of all the pixels by reset control signal phiPGthe transfer elements of the pixel of a line with 1st selected vertical-scanning-signals phiTR are made one. The signal charge accumulated in photo-diode PD is transmitted to the

gate of amplifier QA by thisand the gate voltage of this amplifier QA changes with it corresponding to a signal. Amplifier QA is operated as a source followerthis voltage is outputted to sequence line LVthe horizontal scanning circuit 9 is scanned as mentioned aboveand it reads to the sequential exterior.

[0046]Drawing 3 shows an usable dynamic shift register's composition to the horizontal scanning circuit and vertical scanning circuit of a solid state camera concerning this invention. The dynamic shift register of drawing 3 is created using a CMOS processand shows the example which uses what is called a clocked inverter activated one by one by the clock pulse.

[0047]In the dynamic shift register of drawing 3For exampletwo PMOS transistors P1 and P2 and two NMOS transistors N2 and N1 by which the series connection was carried out between positive power-supply-voltage V_{DD} and negative power-supply-voltage V_{SS} constitute one step of clocked inverter. PMOS transistor P3P4 and NMOS transistor N4and N3 constitute the 2nd step of clocked inverterPMOS transistor P5P6 and two NMOS transistors N6and N5 constitute the 3rd step of clocked invertertwo PMOS transistors P7and P8 and two NMOS transistors N8 and N7 constitute the 4th step of clocked inverterand it is the same as that of the following.

[0048]P2N2and the 2nd step constitute P8N8and a ********** CMOS inverter from P6N6and the 4th step from the PMOS transistor and NMOS transistor which are located in the center in the clocked inverter of each circuit stagesfor examplethe 1st stepin P4N4and the 3rd step. The transistor connected between each CMOS inverterpower supply $V_{DD}$and V_{SS} is a transistor for control for activating these CMOS inverters.

[0049]The gate of PMOS transistor P1P5and -- is connected to internal clock signal line CP1 among these transistors for controland the gate of PMOS transistor P3P7and -- is connected to internal clock signal line CP2. The gate of the transistor N1 for control of other electric conduction typei.e.an NMOS transistorN5and -- is connected to internal clock signal line CN1and the gate is connected to other internal clock signal line CN2 of NMOS transistor N3N7and --.

[0050]Start pulse phiST is supplied to the gate of each transistors P2 and N2 which constitute the 1st step of CMOS inverter. The output of the 1st step of CMOS inverter The input of the 2nd step of CMOS inverterThat isit is connected to the gate of the transistor P4 and the

transistor N4the output of the 2nd step of CMOS inverter is connected to the output of the 3rd step of CMOS inverterand the output of the 3rd step of CMOS inverter is connected to the input of the 4th step of CMOS inverter one by one.
[0051]The dynamic shift register of drawing 3 had further inverter INV2 which constitutes a simultaneous activation circuitOR gateOR1and OR2and has two more inverter INV3 and INV4. Initialization-pulses phiINT is supplied to each one input of OR gates OR1 and OR2. As for the input of another side of OR gate OR1clock pulse phiCK is suppliedand the signal with which the input of another side of other OR gate OR2 reversed clock pulse phiCK by inverter INV2 is supplied. It is connected to the aforementioned internal clock signal line CN2and the output of OR gate OR1 is connected to internal clock signal line CP2 via inverter INV4. It is connected to internal clock signal line CN1and the output of OR gate OR2 is connected to internal clock signal line CP1 via inverter INV3.
[0052]In the dynamic shift register who has the above compositionwhen initialization-pulses phiINT is the low (L) levelclock pulse phiCK occurs in the output of OR gate OR1and the clock pulse which reversed clock pulse phiCK is supplied to the output of OR gate OR2. Thereforewhen clock pulse phiCK is the high (H) levelin internal clock signal line CN2H level and internal clock signal line CP2 becomes L leveland the transistor P3P7-- and N3N7and -- become one. On the other handwhen clock signal phiCK is L levelthe output of OR gate OR2 serves as H leveland the transistor P1P5-- and N1N5and -- become one. Thereforethe 1st inverter and 2nd inverter of each circuit stages are activated by turns by clock signal phiCKand start pulse phiST is shifted one by one to following circuit stages.
[0053]on the other hand -- if initialization-pulses phiINT is used as H level -- the level of clock pulse phiCK -- both the outputs of OR gates OR1 and OR2 serve as H level irrespective of how. Thereforeboth internal clock signal line CN1 and CN2 are set to H leveland both internal clock signal line CP1 and CP2 are set to L level. For this reasonthe transistor P1 for control of all the clocked invertersP3P5P7-- and N1N3N5N7and -- become one simultaneously. That isall the clocked inverters are activated simultaneously.
[0054]Regardless of clock pulse phiCKit is reversed with each inverterand input signal phiST is high-speed and is transmitted to a latter circuit by this. Thereforeif start pulse phiST is used as L levelall also of the output S1 of all the circuit stagesS2and -- will be set to L leveland if

start pulse phiST is used as H levelthe output S1 of all the circuit stagesS2and -- will be set to H level. That isthe output to all the circuit stages or desired circuit stages can be set or preset almost in instant. Since all circuits are in an active stateit is stabilized and they can also continue reset or a preset state for a long time. The time delay of the clocked inverter used for the usual solid state cameraUsuallyit is several or less nanosecondseven if there are 1000 steps of clocked inverterstransfer of data will be possible in several or less microseconds from an input stage to a final stageand reset or presetting of each circuit stages can be performed mostly in an instant.

[0055]Drawing 4 shows other examples of composition of a dynamic shift register which can be used for the solid state camera of this invention. The dynamic shift register of drawing 4 has two CMOS inverters for every circuit stages. That isthe 1st circuit stages have the 1st CMOS inverter that consists of PMOS transistor P11 and NMOS transistor N11and the 2nd CMOS inverter that consists of PMOS transistor P12 and NMOS transistor N12. The 2nd circuit stages are provided with the 1st CMOS inverter that consists of PMOS transistor P13 and NMOS transistor N13and the 2nd CMOS inverter that consists of PMOS transistor P14 and NMOS transistor N14and are the same as that of the following. Cascade connection of each inverter is carried out one by one via the transmission gate. Namelythe output of the inverter which consists of the transistors P11 and N11 is connected to the input of the inverter which consists of the transistors P12 and N12 via the 1st transmission gate T1The output of the transistor P12 and the inverter which consists of N12 is connected to the input of the transistor P13 and the inverter which consists of N13 via the 2nd transmission gate T2It is connected to the input of the transistor P14 and the inverter which consists of N14 via 3rd transmission gate T3and the output of the transistor P13 and the inverter which consists of N13 is the same as that of the following.

[0056]A gate by the side of the transmission gate T1T3and a PMOS transistor of -- is connected to internal clock signal line CP1and a gate of an NMOS transistor is connected to internal clock signal line CN1. A gate of a PMOS transistor of the transmission gate T2T4and -- is connected to internal clock line CP2and a gate of an NMOS transistor is connected to internal clock signal line CN2.

[0057]A dynamic shift register of drawing 4 has a simultaneous activation circuit which consists of inverter

INV2OR gateOR1and OR2 like a thing of drawing 3It has OR gateOR1inverter INV4 which reverse an output of OR2respectively and are supplied to internal clock signal line CP2 and CP1and INV3. An output of OR gateOR1 and OR2 is connected to internal clock signal line CN2 and CN1 again.

[0058]In the dynamic shift register of drawing 4when initialization-pulses phiINT is L levelthe reversal clock pulse in which the output of OR gates OR1 and OR2 reversed clock pulse phiCK and this clock pulse phiCKrespectively is outputted. These clock pulse phiCK and the reversal clock pulse of those are supplied to the internal clock signal lines CN2 and CN1respectively. Inverter INV4 and INV3 are further reversedrespectivelyand clock pulse phiCK outputted from OR gateOR1 and OR2respectively and its reversal clock pulse are supplied to internal clock signal line CP2 and CP1respectively. That isclock pulse phiCK is supplied for the clock pulse which reversed clock signal phiCK to internal clock signal line CP2 to internal clock signal line CP1.

[0059]Thereforewhen clock pulse phiCK is H levelthe transmission gate T2T4and -- conductand when clock pulse phiCK is L levelthe transmission gate T1T3and -- conduct. That isthe transmission gate T1T2T3T4and -- are made conduction and non-conduction by turns by clock signal phiCK. Start pulse phiST is transmitted one by one to following circuit stages like well-known by thisand a shift action is performed.

[0060]On the other handwhen initialization-pulses phiINT is H levelboth the outputs of OR gateOR1 and OR2 serve as H level irrespective of the level of clock pulse phiCK. For this reasoninternal clock signal line CN1 and CN2 are set to H level and internal clock signal line CP1both CP2 [both] are set to L leveland all the transmission gates T1T2T3T4and -- conduct. That iscascade connection of the inverter of all the circuit stages will be carried out directly. Thereforewhile start pulse phiST is reversed one by onedirect transmission is carried out by each inverter. Thereforeit becomes possible to reset or preset each circuit stages in an instant also in the circuit of drawing 4.

[0061]In above-mentioned explanationalthough explained per two kinds of things as a dynamic shift registerit is clear to this invention that the dynamic shift register of various forms can be used. That iseach circuit stages comprise 1 set of two-step dynamic form inverter circuitsand substantiallyin an active stateone of the two

can apply this inventionif another side is a dynamic shift register of form who transmits an input signal to following circuit stages one by one as an inactive state substantially. 1 set of two-step dynamic form inverters can be simultaneously activated in these casesan input signal can be transmitted to the circuit stages of direct succession over two or more circuit stagesand reset and presetting can be made to perform in an instant compulsorily.

[0062]Nextdrawing 5 shows the circuitry of the solid state camera concerning another enforcement aspect of this invention. Also in drawing 5the same portion as said drawing 1 is shown by the same reference number. In the solid state camera of drawing 5each sequence line LV1 in the solid state camera of said drawing 2LV2and LV3 are connected to the predetermined bias voltage VPU via switch element QPU1 which comprises a MOS transistor for pull-upetc.respectivelyQPU2and QPU3. The gate of each switch element QPU1QPU2and QPU3 is constituted so that it may be connected in common and predetermined control signal phiPU can be supplied. Even if the gate of amplifier QA is the read voltage VGH of amplifier QAlet bias voltage VPU be the voltage which this amplifier QA cuts off. Other portions are the same as the circuit of drawing 2and the same reference number and reference mark are given to the same portion.

[0063]In resetting a pixel in the solid state camera of drawing 5like the case of drawing 2the whole page of the vertical scanning circuit 5 is presetthe 1st vertical scanning circuit phiTR1 - TR3 are added to the switch QT for transmission of all the pixelsand it considers this switch QT for transmission as one. Control signal phiPG is added and the reset switch QRST of all the pixels is made one. Let voltage of the 2nd vertical-scanning-signals phiRD1 - phiRD3 be the read voltage VGH of amplifier QA of each picture element part at this time.

[0064]Bias of each sequence lines LV1-LV3 is carried out to said bias voltage VPU by control signal phiPU by considering the switch element QPU for pull-up of each sequence as one at this time. As mentioned aboveeven if the gate of amplifier QA is the read voltage VGHlet this bias voltage VPU be the voltage which amplifier QA cuts off. By thiswhere amplifier QA is cut offthe residual charge of photo-diode PD is emitted via the transfer elements QT and reset element QRSTand reset of a pixel is performed. And photo-diode PD is reset in this case by the state where reverse bias was carried out to the read voltage VGH of

amplifier QA. Howeverby the switch element QPU for pull-upthe source voltage of each amplifier QA is said bias voltage VPUand current does not flow into amplifier QA. That isthe excessive rush current at the time of reset can be prevented. When reading a signalwhere the switch element QPU for pull-up is considered as cutoffit carries out like the case of the solid state camera of said drawing 2.
[0065]In the solid state camera of above-mentioned drawing 2 and drawing 5it is desirable to constitute as the characteristic of the photo detector of each pixelso that perfect depletion may be formed at the time of reset. Howeverif the characteristic of JFET which constitutes amplifier QA if a production process condition is set up constitute such a photo detector may not be enough and the characteristic of JFET is thought as important converselyperfect depletion-ization of a photo detector may be unable to be attained. Thereforewhen it is desirable to have composition of said drawing 2and difficult [coexistence]when both the JFET characteristics of the photo-diode of a photo detector and an amplifier are compatible with the desired characteristicor impossibleit is desirable to have composition of drawing 5.
[0066]
[Working example]In the solid state camera in above-mentioned drawing 2 and drawing 5the voltage of each power supply and a signal is specifically set up as followsand a high result is obtained. That isamplifier QA of each of said pixel sets to read voltage VGH=-1V which is turned on and activated on condition of power-supply-voltage VDD=5V and VEE=0V. And for example-3V may be sufficient as the voltage VGL of 2nd vertical-scanning-signals phiRD supplied to the drain of the reset element of each pixel at the time of the reset in the composition of said drawing 2. Bias voltage VPU for cutting off each pixel in the composition of said drawing 5 is made into the voltage (for examplemore than +1V) which this amplifier QA cuts off even if the gate voltage of amplifier QA is VGH=-1V.
[0067]
[Effect of the Invention]As mentioned abovesince according to this invention it constituted in the solid state camera so that a photo detector might be resetwhere the amplifier of each pixel is cut off when resettingAlso when resetting simultaneously the solid state camera smell all pixel containing many pixelsexcessive rush current can be prevented from occurring. Thereforethe fall of the reliability of the solid state camera by rush current can be preventedand it enables a solid state camera to prevent

having an adverse effect on a solid state cameraand to demonstrate original performance by the voltage variation of each part of the inside of a chip by rush current. All the pixel simultaneous reset can use such a solid state camera for a required electronic "still" camera etc. at the moment of turning off the shutterfor exampleand it can obtain a good result.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing the composition of the outline of the solid state image pickup device concerning this invention.
[Drawing 2]It is an electric diagram showing the detailed composition of the solid state camera concerning a 1st embodiment of this invention.
[Drawing 3]It is an electric diagram showing the composition of a shift register usable to the scanning circuit of the solid state camera concerning this invention.
[Drawing 4]It is an electric diagram showing other composition of a shift register usable to the scanning circuit of the solid state image pickup device concerning this invention.
[Drawing 5]It is an electric diagram showing the detailed composition of the solid state image pickup device concerning a 2nd embodiment of this invention.
[Drawing 6]It is an electric diagram showing the composition of the conventional solid state camera.
[Explanations of letters or numerals]
1 Pixel
3 Picture element part
5 vertical scanning circuit (VSR)
7 Level read section
9 horizontal scanning circuit (HSR)
PD11--PD33 Photo-diode
QT11--QT33 Transfer elements
QA11--QA33 Amplifier
QRST11--QRST33 reset element
CSV1--CSV3 Constant current source
QTC1--QTC3 read-out gate transistors
CT1--CT3 Capacity for accumulation
QH1--QH3 Switch element for level read-out
QPU1--QPU3 Switch element for pull-up